

What is Claimed is:

1 1. An apparatus for compensating for offset and drift of offset in an
2 amplifier, comprising:
3 an amplifier circuit having metal oxide semiconductor transistors in an
4 input stage thereof and including a node responsive to a bias to change the
5 offset of the amplifier circuit;
6 an offset digital-to-analog converter providing a first programmable
7 bias corresponding to an offset of the amplifier circuit; and
8 a drift digital-to-analog converter providing a second programmable
9 bias corresponding to a drift of the offset of the amplifier circuit;
10 the first programmable bias and the second programmable bias being
11 combined and coupled to the node.

1 2. A method for compensating for offset and drift of offset in an amplifier
2 circuit having metal oxide semiconductor transistors in an input stage thereof
3 and including a node responsive to a bias to change the offset of the amplifier
4 circuit, comprising the steps of:
5 providing a first programmable bias corresponding to an offset of the
6 amplifier circuit;
7 providing a second programmable bias corresponding to a drift of the
8 offset of the amplifier circuit;
9 combining the first programmable bias and the second programmable
10 bias and coupling the combined biases to the node.

1 3. An apparatus for compensating for offset and drift of offset in an
2 amplifier, comprising:
3 an amplifier circuit having metal oxide semiconductor transistors in an
4 input stage thereof and including a node responsive to a bias to change the
5 offset of the amplifier circuit;

6 a first programmable offset/drift generator capable of sourcing a first
7 bias to the amplifier node compensating for a first portion of the offset and a
8 first portion of the drift of the offset of the amplifier circuit; and

9 a second programmable offset/drift generator capable of sourcing a
10 second bias to the amplifier node compensating for a second portion of the
11 offset and a second portion of the drift of the offset of the amplifier circuit,
12 wherein the rate of drift compensation with temperature of the second bias is
13 different from the rate of compensation of the second bias, such that by
14 suitable programming of the first and second programmable offset/drift
15 generators the compensation of the offset and the offset of the drift of the
16 amplifier circuit may be optimized.

1 4. A method for compensating for offset and drift of offset in an amplifier
2 circuit having metal oxide semiconductor transistors in an input stage thereof
3 and including a node responsive to a bias to change the offset of the amplifier
4 circuit, comprising the steps of:

5 providing a first programmable bias to the amplifier node compensating
6 for a first portion of the offset and a first portion of the drift of the offset of the
7 amplifier circuit; and

8 providing a second programmable bias to the amplifier node
9 compensating for a second portion of the offset and a second portion of the
10 drift of the offset of the amplifier circuit; and

11 controlling the rate of drift compensation with temperature of the first
12 bias and the second bias such that the second bias is different from the rate
13 of compensation of the second bias and the compensation of the offset and
14 the offset of the drift of the amplifier circuit is optimized.

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1 5. A method for compensating for offset and drift of offset in an amplifier
2 circuit having metal oxide semiconductor transistors in an input stage thereof

3 and including a node responsive to a bias to change the offset of the amplifier
4 circuit, comprising the steps of:
5 measuring a first offset error at a first temperature;
6 storing the first offset error in a first memory;
7 measuring a second offset error at a second temperature;
8 storing the second offset error in the first memory;
9 computing drift and offset at the first temperature, based on the first
10 offset error;
11 computing an offset compensation code;
12 storing the offset compensation code in a second, non-volatile
13 memory;
14 computing an offset drift compensation code;
15 storing the offset drift compensation code in the second memory; and
16 upon activation of the amplifier circuit:
17 retrieving the offset compensation code and the offset drift
18 compensation code;
19 responsive to the retrieved offset compensation code, providing a first
20 programmable bias corresponding to an offset of the amplifier circuit;
21 responsive to the retrieved offset drift compensation code, providing a
22 second programmable bias corresponding to a drift of the offset of the
23 amplifier circuit;
24 combining the first programmable bias and the second programmable
25 bias and coupling the combined biases to the node.